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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/430,366	10/28/1999	MARK T. RAMSBY	M-7523-US	7206

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23

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No. 09/430,366	Applicant(s) Ramsbey et al.	Examiner Jack Chen Art Unit 2813
		

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on Nov 12, 2002
- 2a) This action is FINAL. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1, 3-7, 9-12, 14, 15, and 23 is/are pending in the application.
- 4a) Of the above, claim(s) _____ is/are withdrawn from consideration.
- 5) Claim(s) _____ is/are allowed.
- 6) Claim(s) 1, 3-7, 9-12, 14, 15, and 23 is/are rejected.
- 7) Claim(s) _____ is/are objected to.
- 8) Claims _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on _____ is/are a) accepted or b) objected to by the Examiner. Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) The proposed drawing correction filed on _____ is: a) approved b) disapproved by the Examiner. If approved, corrected drawings are required in reply to this Office action.
- 12) The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) All b) Some* c) None of:

1. Certified copies of the priority documents have been received.
2. Certified copies of the priority documents have been received in Application No. _____.
3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

*See the attached detailed Office action for a list of the certified copies not received.

- 14) Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).
- a) The translation of the foreign language provisional application has been received.
- 15) Acknowledgement is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) Notice of References Cited (PTO-892)
- 2) Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) Information Disclosure Statement(s) (PTO-1449) Paper No(s). _____
- 4) Interview Summary (PTO-413) Paper No(s). _____
- 5) Notice of Informal Patent Application (PTO-152)
- 6) Other: _____

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DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on November 12, 2002 has been entered.

Claim Objections

2. Claims 1, 3-6, 7, 9-12, 14-15 and 23 are objected to because of the following informalities:

Re claim 1, line 5, the term “layerand” should change to --layer and--.

Re claim 1, line 6, the phrase “the insulator layer forming” should change to --the insulator layer is formed--.

Re claim 7, line 3, the phrase “the tunnel oxide” should change to --the tunnel oxide layer--.

Re claim 23, line 6, the phrase “the insulator layer of high quality oxide on” should change to --the insulator layer of high quality oxide is formed on--.

Appropriate correction is required.

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Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103© and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

4. Claims 1, 3, 5, 6, 7, 9, 11, 12 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wu, U.S./6,033,956 or Mitchell et al., U.S./4,713,142 in view of Paterson et al., U.S./4,613,956.

Wu discloses a method for forming a semiconductor device having a substrate and a tunnel oxide 202 formed on the substrate, which comprises depositing a floating gate layer on the tunnel oxide to a first thickness; etching the floating gate layer, to provide a floating gate 204; depositing an insulator layer of oxide 210 (CVD oxide, inherently shows the oxide is the high temperature oxide and not limited to any particular type CVD methods [i.e., LPCVD, PECVD,

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etc.], which produces the high temperature/quality oxide; furthermore, on page 4, lines 27-29 of the instant application, applicant discloses that any other dielectric material will provide the same results. In addition, the disclosure fails to mention the criticality of the LPCVD process) directly on exposed portions of the tunnel oxide and the floating gate such that the insulator layer has a thickness that is greater than the first thickness (inherently shows using the insulator layer to prevent charge leaking from the floating gate, see fig. 2C); polishing the insulator layer to provide a planar surface that exposes a top surface of the floating gate and the insulator layer (fig. 2c); and depositing a dielectric layer 214 on the planar surface directly over the exposed top surface of the floating gate and the insulator layer, see figs. 1-4G, cols. 1-6.

Mitchell et al. also disclose a method for forming a semiconductor device having a substrate and a tunnel oxide 32 formed on the substrate, which comprises depositing a floating gate layer on the tunnel oxide to a first thickness; etching the floating gate layer, to provide a floating gate 33 (fig. 2a); depositing an insulator layer (note: both layers 36 and 37 can be considered as an insulating layer) of oxide 36 and 37 (CVD oxide, inherently shows the oxide is the high temperature oxide and is not limited to any particular type CVD methods [i.e., LPCVD, PECVD, etc.], which produces the high temperature/quality oxide; furthermore, on page 4, lines 27-29 of the instant application, applicant discloses that any other dielectric material will provide the same results. In addition, the disclosure fails to mention the criticality of the LPCVD process) directly on exposed portions of the tunnel oxide and the floating gate such that the insulator layer has a thickness that is greater than the first thickness (fig. 2c); polishing the insulator layer to

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provide a planar surface that exposes a top surface of the floating gate and the insulator layer (fig. 2d); and depositing a dielectric layer 39 on the planar surface directly over the exposed top surface of the floating gate and the insulator layer, see figs. 1-5, cols. 1-6.

However, Wu and Mitchell et al. are silent to LPCVD oxide. Paterson et al. discloses a method for forming a semiconductor device, which includes depositing the high temperature/quality oxide on the floating gate by LPCVD in order to provide high uniformity and a highly doped floating gate (col. 3, lines 65-col. 4, lines 6 and col. 4, line 67-col. 5, line 47) and using ONO for the inter-poly dielectric, see figs. 1-8c, cols. 1-10.

Therefore, the subject matter as a whole would have been obvious to one having ordinary skill in the art at the time the invention was made to use LPCVD oxide as taught by Paterson et al. in the method of Wu or Mitchell et al. in order to provide high uniformity and using ONO in order to provide high capacitance. Furthermore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the method of Wu or Mitchell et al. by selecting the suitable thicknesses for the floating gate and the insulator layer, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller*, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955).

5. Claims 4, 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wu, U.S./6,033,956 or Mitchell et al., U.S./4,713,142 taken with Paterson et al., U.S./4,613,956 as

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applied to claims 1, 3, 5, 6, 7, 9, 11, 12 and 23 above, and further in view of Yamagishi et al., U.S./5,808,339.

Wu, Mitchell et al. and Paterson et al. disclosed above. However, Wu, Mitchell et al. and Paterson et al. are silent to polishing the insulator layer by CMP.

Yamagishi et al. (figs. 9A-10D) discloses a method for forming a semiconductor device having a substrate 11 and a tunnel oxide 51 formed on the substrate, which comprises depositing a floating gate layer 53 on the tunnel oxide to a first thickness; etching the floating gate layer, to provide a floating gate 53; depositing an insulator layer of oxide 54 (by CVD) on the substrate and the floating gate such that the insulator layer has a thickness that is greater than the first thickness; polishing (using CMP or etching back; Art recognized equivalents: using CMP or etching back, because these two methods are art-recognized equivalents at the time the invention was made, one of ordinary skill in the art would have found it obvious to substitute one for another) the insulator layer to provide a planar surface that exposes a top surface of the floating gate and the insulator layer (fig. 10A); and depositing a dielectric layer 55 (ONO) on the planar surface directly over the exposed top surface of the floating gate and the insulator layer, see figs. 1-12B, cols. 1-16.

Therefore, the subject matter as a whole would have been obvious to one having ordinary skill in the art at the time the invention was made to use CMP method as taught by Yamagishi et al. in the method of Wu or Mitchell et al taken with Paterson et al. in order to provide a planar surface. Furthermore, using either CMP or etching back method is Art recognized equivalents:

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using CMP or etching back, because these two methods are art-recognized equivalents at the time the invention was made, one of ordinary skill in the art would have found it obvious to substitute one for another.

6. Claims 14-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wu, U.S./6,033,956 or Mitchell et al., U.S./4,713,142 taken with Paterson et al., U.S./4,613,956 as applied to claims 1, 3, 5, 6, 7, 9, 11, 12 and 23 above, and further in view of Applicant's admitted prior art.

Wu, Mitchell et al. and Paterson et al. disclosed above. However, Wu, Mitchell et al. and Paterson et al. are silent to use doped polysilicon or amorphous silicon for the floating gate.

Applicant's admitted prior art teaches using doped polysilicon or doped amorphous silicon for the floating gate, see pages 1-2.

Therefore, the subject matter as a whole would have been obvious to one having ordinary skill in the art at the time the invention was made to use doped polysilicon or amorphous silicon for the floating gate as taught by applicant's admitted prior art in order to increase the conductivity of the floating gate.

7. Claims 1, 3-7, 9-12, 14-15, 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamagishi et al., U.S./5,808,339 or Chan et al., U.S./6,051,467 taken with Sze et al., "ULSI Technology" and in view of Applicant's admitted prior art.

Yamagishi et al. (figs. 9A-10D) discloses a method for forming a semiconductor device having a substrate 11 and a tunnel oxide 51 formed on the substrate, which comprises depositing

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a floating gate layer 53 on the tunnel oxide to a first thickness; etching the floating gate layer, to provide a floating gate 53; depositing an insulator layer of oxide 54 (by CVD) on the substrate and the floating gate such that the insulator layer has a thickness that is greater than the first thickness; polishing the insulator layer to provide a planar surface that exposes a top surface of the floating gate and the insulator layer (fig. 10A); and depositing a dielectric layer 55 on the planar surface directly over the exposed top surface of the floating gate and the insulator layer, see figs. 1-12B, cols. 1-16.

Chan et al. further discloses a method for forming a semiconductor device having a substrate 10 and a tunnel oxide 16 formed on the substrate, which comprises depositing a floating gate layer 18 on the tunnel oxide to a first thickness; etching the floating gate layer, to provide a floating gate 18; depositing an insulator layer of oxide 30 (by CVD methods, i.e., APCVD or PECVD) on the substrate and the floating gate such that the insulator layer has a thickness that is greater than the first thickness; polishing the insulator layer to provide a planar surface that exposes a top surface of the floating gate and the insulator layer (fig. 5); and depositing a dielectric layer on the planar surface directly (layer 32 is an optional layer, which is well known in the art) over the exposed top surface of the floating gate and the insulator layer, see figs. 1-11, cols. 1-8.

However, the above references are silent to forming high temperature oxide by using LPCVD method (Note: during the telephone interview dated on 8/3/2001, applicant admitted that this layer is well known in the art and it is formed by LPCVD process, also see the

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amendment dated on 8/6/2001, furthermore, applicant stated in the specification, other dielectric may used, i.e., see page 3, lines 26-30. In addition, the disclosure fails to mention the criticality of the LPCVD process).

It is well known in the art to form the dielectric by using any CVD process. For example, Sze et al. teaches forming the dielectric by using LPCVD process, such will provide excellent purity and uniformity, conformal step coverage, large wafer capacity, high throughput, etc. Furthermore, it is well known in the art to use doped polysilicon or doped amorphous silicon for the floating gate, such will increase the conductivity of the floating gate. For example, applicant's admitted prior art teaches using doped polysilicon or doped amorphous silicon for the floating gate, see pages 1-2.

Furthermore, the thickness of claims 3 and 9 are considered to involve routine optimization while has been held to be within the level of ordinary skill in the art. As noted in *In re Aller*, the selection of reaction parameters such as energy, dosage, thickness, width; the rate of etching, temperature and concentration would have been obvious:

"Normally, it is to be expected that a change in energy, etching rate, thickness, dosage, temperature, or combination of any of them would be an unpatentable modification.

Under some circumstances, however, changes such as these may impart patentability to a process if the particular ranges claimed produce a new and unexpected result which is different in kind and not merely degree from the results of the prior art...such ranges are termed "critical ranges and the applicant has the burden of proving such criticality....

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More particularly, where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation."

In re Aller 105 USPQ233, 255 (CCPA 1955). See also *In re Waite* 77 USPQ 586 (CCPA 1948); *In re Scherl* 70 USPQ 204 (CCPA 1946); *In re Irmscher* 66 USPQ 314 (CCPA 1945); *In re Norman* 66 USPQ 308 (CCPA 1945); *In re Swenson* 56 USPQ 372 (CCPA 1942); *In re Sola* 25 USPQ 433 (CCPA 1935); *In re Dreyfus* 24 USPQ 52 (CCPA 1934).

Therefore, one of ordinary skill in the requisite art at the time the invention was made would have used any thickness range suitable to the method in process of Yamagishi et al. or Chan et al. taken with Sze et al. and in view of Applicant's admitted prior art in order to optimize the process.

Furthermore, the subject matter as a whole would have been obvious to one having ordinary skill in the art at the time the invention was made to further modify the standard process of Yamagishi et al. or Chan et al. with the teaching of Sze et al. and Applicant's admitted prior art because of the desirability to improve device reliability and performance of the device (also see above); in addition, the subject matter as a whole would have been obvious to one having ordinary skill in the art at the time the invention was made to use LPCVD oxide as matter of design choice since applicant has not disclosed that LPCVD method solves any stated problems or is for any particular purpose and it appears that the invention would perform equally well with any CVD processes.

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Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jack Chen whose telephone number is (703) 308-5838. The examiner can normally be reached on Monday-Friday (alternate Monday off) from 8:30 am to 6:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead, Jr., can be reached on (703)308-4940. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9318 for regular communications and 703-872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)308-0956.

Jack Chen


JACK CHEN
PATENT EXAMINER

December 2, 2002